CLAIMS

What is claimed is:

1. A heterojunction bipolar transistor (HBT), comprising:

a collector;

an emitter; and

a base located between the collector and the emitter, the base including a layer of gallium arsenide antimonide (GaAsSb) less than 49 nanometers (nm) thick.

2. The HBT of claim 1, wherein the gallium arsenide antimonide of the base has an arsenic (As) fraction in a range from about 50% to about 51%.

3. The HBT of claim 1, wherein the gallium arsenide antimonide of the base has an arsenic (As) fraction in a range from about 50% to about 65%.

4. The HBT of claim 1, wherein the gallium arsenide antimonide of the base has an arsenic (As) fraction in a range from about 50% to about 60%.

5. The HBT of claim 1, wherein the gallium arsenide antimonide of the base has an arsenic (As) fraction in a range from about 54% to about 56%.

6. The HBT of claim 1, wherein the gallium arsenide antimonide of the base has an arsenic (As) fraction of approximately 55%.

7. The HBT of claim 1, wherein the base layer of GaAsSb is less than 20 nm thick.

8. The HBT of claim 1, wherein the base layer of GaAsSb is strained so that its lattice constant conforms to the lattice constant of the collector and the emitter.

9. The HBT of claim 1, wherein the base layer of GaAsSb is doped with beryllium (Be) at a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

10. The HBT of claim 1, wherein the base layer of GaAsSb is doped with carbon (C) at a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

11. The HBT of claim 7, wherein the base layer of GaAsSb is doped with carbon (C) at a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

12. A method for making a heterojunction bipolar transistor (HBT), the method comprising:

forming a collector;

forming an emitter; and

forming a base located between the collector and the emitter, the base including a layer of gallium arsenide antimonide (GaAsSb) less than 49 nanometers (nm) thick.

13. The method of claim 12, wherein the base is formed of gallium arsenide antimonide having an arsenic (As) fraction in a range from about 50% to about 51%.

14. The method of claim 12, wherein the base is formed of gallium arsenide antimonide having an arsenic (As) fraction in a range from about 50% to about 65%.

15. The method of claim 12, wherein the base is formed gallium arsenide antimonide having an arsenic (As) fraction in a range from about 50% to about 60%.

16. The method of claim 12, wherein the base is formed of gallium arsenide antimonide having an arsenic (As) fraction in a range from about 54% to about 56%.

17. The method of claim 12, wherein the base is formed of gallium arsenide antimonide having an arsenic (As) fraction of approximately 55%.

18. The method of claim 12, wherein the base layer of GaAsSb is less than 20 nm thick.

19. The method of claim 12, further comprising the step of straining the base layer of GaAsSb so that its lattice constant conforms to the lattice constant of the collector and the emitter.

20. The method of claim 12, further comprising the step of doping the base layer of GaAsSb with beryllium (Be) at a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

21. The method of claim 12, further comprising the step of doping the base layer of GaAsSb with carbon (C) at a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

22. A heterojunction bipolar transistor (HBT), comprising:

a collector including indium phosphide (InP);

an emitter including InP; and

a base including a layer of gallium arsenide antimonide (GaAsSb) located between the collector and the emitter, the base layer being less than 49 nanometers (nm) thick and having an arsenic fraction of approximately 55% and a doping concentration of between approximately $6x10^{19}$ and $4x10^{20}$ acceptors/cm^3.

23. The HBT of claim 22, wherein the base layer of GaAsSb is less than 20 nm thick.

24. The HBT of claim 22, wherein the base layer of GaAsSb is strained so that its lattice constant conforms to the lattice constant of the collector and the emitter.

25. The HBT of claim 22, where the HBT is configured as an npn transistor.